

Abstract

A distributed shared memory system having a memory access request transaction queue having a plurality of queue slots prevents occurrences of deadlocks. The distributed shared memory system is implemented in a networked multiprocessor computing system, and includes, in each coherency controller of each of the memories in the system, a mechanism to reserve at least one slot of the memory access request transaction queue for exclusive processing of processor return (PR) transactions to provide an uninterrupted processing of PR transactions. The number of blocking (BL) transaction is limited to a number less than available slots. The distributed shared memory system also includes a distributed memory return transaction queue that allows each of entries in the memory access request transaction queue to add a plurality of memory return transactions per clock cycle.